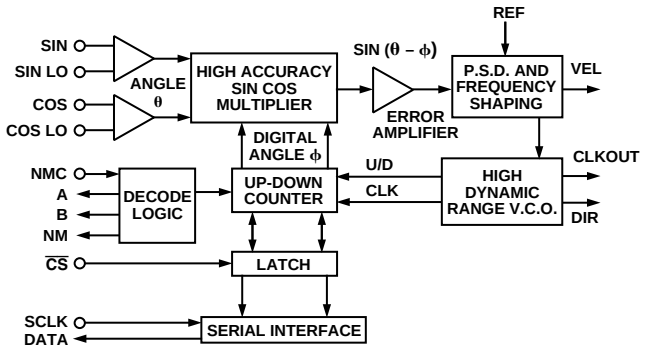
Low Cost, Complete 12-Bit Resolver-to-Digital Converter

AD2S90

FEATURES
Complete Monolithic Resolver-to-Digital Converter
Incremental Encoder Emulation (1024-Line)
Absolute Serial Data (12-Bit)
Differential Inputs
12-Bit Resolution
Industrial Temperature Range
20-Lead PLCC
Low Power (50 mW)

APPLICATIONS
Industrial Motor Control
Servo Motor Control
Industrial Gauging
Encoder Emulation
Automotive Motion Sensing and Control
Factory Automation
Limit Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S90 is a complete 12-bit resolution tracking resolver-to-digital converter. No external components are required to operate the device.

The converter accepts 2 V rms ± 10% input signals in the range 3 kHz–20 kHz on the SIN, COS and REF inputs. A Type II servo loop is employed to track the inputs and convert the input SIN and COS information into a digital representation of the input angle. The bandwidth of the converter is set internally at 1 kHz within the tolerances of the device. The guaranteed maximum tracking rate is 500 rps.

Angular position output information is available in two forms, absolute serial binary and incremental A quad B.

The absolute serial binary output is 12-bit (1 in 4096). The data output pin is high impedance when Chip Select $\overline{CS}$ is logic HI. This allows the connection of multiple converters onto a common bus. Absolute angular information in serial pure binary form is accessed by $\overline{CS}$ followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz.

The encoder emulation outputs A, B and NM continuously produce signals equivalent to a 1024 line encoder. When decoded this corresponds to 12 bits of resolution. Three common north marker pulsewidths are selected via a single pin (NMC).

An analog velocity output signal provides a representation of velocity from a rotating resolver shaft traveling in either a clockwise or counterclockwise direction.

The AD2S90 operates on ±5 V dc ± 5% power supplies and is fabricated on Analog Devices' Linear Compatible CMOS process (LC^2MOS). LC^2MOS is a mixed technology process that combines precision bipolar circuits with low power CMOS logic circuits.

PRODUCT HIGHLIGHTS

Complete Resolver-Digital Interface. The AD2S90 provides the complete solution for digitizing resolver signals (12-bit resolution) without the need for external components.

Dual Format Position Data. Incremental encoder emulation in standard A QUAD B format with selectable North Marker width. Absolute serial 12-bit angular binary position data accessed via simple 3-wire interface.

Single High Accuracy Grade in Low Cost Package. ±10.6 arc minutes of angular accuracy available in a 20-lead PLCC.

Low Power. Typically 50 mW power consumption.

REV. D

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AD2S90–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Condition
SIGNAL INPUTS					
Voltage Amplitude	1.8	2.0	2.2	V rms	Sinusoidal Waveforms, Differential SIN to SINLO, COS to COSLO
Frequency	3		20	kHz	
Input Bias Current			100	nA	V_{IN} = 2 ± 10% V rms
Input Impedance	1.0			MΩ	V_{IN} = 2 ± 10% V rms
Common-Mode Volts[1]			100	mV peak	CMV @ SINLO, COSLO w.r.t.
CMRR	60			dB	AGND @ 10 kHz
REFERENCE INPUT					
Voltage Amplitude	1.8	2.0	3.35	V rms	Sinusoidal Waveform
Frequency	3		20	kHz	
Input Bias Current			100	nA	
Input Impedance	100			kΩ	
Permissible Phase Shift	–10		+10	Degrees	Relative to SIN, COS Inputs
CONVERTER DYNAMICS					
Bandwidth	700	840	1000	Hz	
Maximum Tracking Rate	500			rps	
Maximum VCO Rate (CLKOUT)	2.048			MHz	
Settling Time					
1° Step		2	7	ms	
179° Step			20	ms	
ACCURACY					
Angular Accuracy[2]			±10.6 + 1 LSB	arc min	
Repeatability[3]			1	LSB	
VELOCITY OUTPUT					
Scaling	120	150	180	rps/V dc	
Output Voltage at 500 rps	±2.78	±3.33	±4.17	V dc	
Load Drive Capability			±250	µA	V_{OUT} = ±2.5 V dc (typ), $R_L \geq$ 10 kΩ
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage (V_{INH})	3.5			V dc	V_{DD} = +5 V dc, V_{SS} = –5 V dc
Input Low Voltage (V_{INL})			1.5	V dc	V_{DD} = +5 V dc, V_{SS} = –5 V dc
Input Current (I_{IN})			10	µA	
Input Capacitance			10	pF	
LOGIC OUTPUTS DATA, A, B,[4]					
NM, CLKOUT, DIR					V_{DD} = +5 V dc, V_{SS} = –5 V dc
Output High Voltage	4.0			V dc	I_{OH} = 1 mA
Output Low Voltage			1.0	V dc	I_{OL} = 1 mA
			0.4	V dc	I_{OL} = 400 µA
SERIAL CLOCK (SCLK)					
SCLK Input Rate			2	MHz	
NORTH MARKER CONTROL (NMC)					
90°	+4.75	+5.0	+5.25	V dc	North Marker Width Relative to
180°	–0.75	DGND	+0.75	V dc	"A" Cycle
360°	–4.75	–5.0	–5.25	V dc	
POWER SUPPLIES					
V_{DD}	+4.75	+5.00	+5.25	V dc	
V_{SS}	–4.75	–5.00	–5.25	V dc	
I_{DD}			10	mA	
I_{SS}			10	mA	

NOTES
[1]If the tolerance on signal inputs = ±5%, then CMV = 200 mV.
[2]1 LSB = 5.3 arc minute.
[3]Specified at constant temperature.
[4]Output load drive capability.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

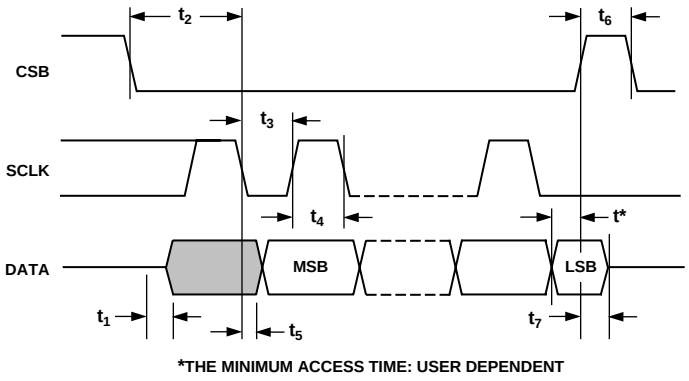


Figure 1. Serial Interface

NOTES
[1]Timing data are not 100% production tested. Sample tested at +25°C only to ensure conformance to data sheet limits. Logic output timing tests carried out using 10 pF, 100 kΩ load.
[2]Capacitance of data pin in high impedance state = 15 pF.

Parameter	AD2S90	Units	Test Conditions/Notes
t_1	150	ns max	$\overline{CS}$ to DATA Enable
t_2[1]	600	ns min	$\overline{CS}$ to 1st SCLK Negative Edge
t_3	250	ns min	SCLK Low Pulse
t_4	250	ns min	SCLK High Pulse
t_5	100	ns max	SCLK Negative Edge to DATA Valid
t_6	600	ns min	$\overline{CS}$ High Pulsewidth
t_7	150	ns max	$\overline{CS}$ High to DATA High Z (Bus Relinquish)

NOTE
[1]SCLK can only be applied after t_2 has elapsed.

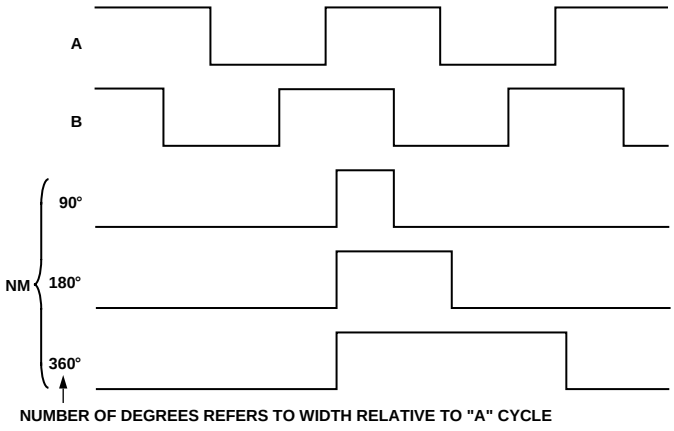


Figure 2. Incremental Encoder

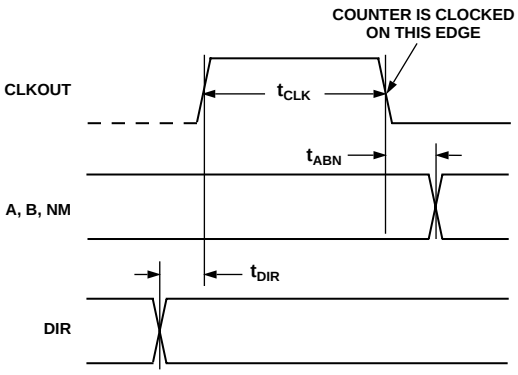


Figure 3. DIR/CLKOUT/A, B and NM Timing

Parameter	AD2S90 Min	AD2S90 Max	Units	Test Conditions/Notes
t_{DIR}		200	ns	DIR to CLKOUT Positive Edge
t_{CLK}	250	400	ns	CLKOUT Pulsewidth
t_{ABN}		250	ns	CLKOUT Negative Edge to A, B and NM Transition

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($V_{DD} - V_{SS}$) . . . . . ±5 V dc ± 5%
Analog Input Voltage (SIN, COS & REF) . . . . . 2 V rms ± 10%
Signal and Reference Harmonic Distortion 10%
Phase Shift between Signal and Reference . . . . . ±10°
Ambient Operating Temperature Range
Industrial (AP) . . . . . –40°C to +85°C

ABSOLUTE MAXIMUM RATINGS*

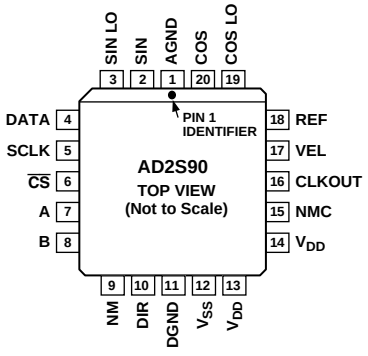
V_{DD} to AGND . . . . . –0.3 V dc to +7.0 V dc
V_{SS} to AGND . . . . . +0.3 V dc to –7.0 V dc
AGND to DGND . . . . . –0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND
REF . . . . . V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
SIN, SIN LO . . . . . V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
COS, COS LO . . . . . V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
Analog Output to AGND
VEL . . . . . V_{SS} to V_{DD}
Digital Inputs to DGND, CSB,
SCLK, RES . . . . . –0.3 V dc to V_{DD} + 0.3 V dc
Digital Outputs to DGND, NM, A, B,
DIR, CLKOUT DATA . . . . . –0.3 V dc to V_{DD} + 0.3 V dc
Operating Temperature Range
Industrial (AP) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C
Power Dissipation to +75°C . . . . . 300 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Option
AD2S90AP	–40°C to +85°C	10.6 arc min	P-20A

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin No.	Mnemonic	Function
1	AGND	Analog ground, reference ground.
2	SIN	SIN channel noninverting input connect to resolver SIN HI output. SIN to SIN LO = 2 V rms ± 10%.
3	SIN LO	SIN channel inverting input connect to resolver SIN LO.
4	DATA	Serial interface data output. High impedance with $\overline{CS}$ = HI. Enabled by $\overline{CS}$ = 0.
5	SCLK	Serial interface clock. Data is clocked out on "first" negative edge of SCLK after a LO transition on $\overline{CS}$. 12 SCLK pulses to clock data out.
6	$\overline{CS}$	Chip select. Active LO. Logic LO transition enables DATA output.
7	A	Encoder A output.
8	B	Encoder B output.
9	NM	Encoder North Marker emulation output. Pulse triggered as code passes through zero. Three common pulsewidths available.
10	DIR	Indicates direction of rotation of input. Logic HI = increasing angular rotation. Logic LO = decreasing angular rotation.
11	DGND	Digital power ground return.
12	V_{SS}	Negative power supply, –5 V dc ± 5%.
13	V_{DD}	Positive power supply, +5 V dc ± 5%.
14	V_{DD}	Positive power supply, +5 V dc ± 5%. Must be connected to Pin 13.
15	NMC	North marker width control. Internally pulled HI via 50 kΩ nominal.
16	CLKOUT	Internal VCO clock output. Indicates angular velocity of input signals. Max nominal rate = 1.536 MHz. CLKOUT is a 300 ns positive pulse.
17	VEL	Indicates angular velocity of input signals. Positive voltage w.r.t. AGND indicates increasing angle. FSD = 375 rps.
18	REF	Converter reference input. Normally derived from resolver primary excitation. REF = 2 V rms nominal. Phase shift w.r.t. COS and SIN = ±10° max
19	COS LO	COS channel inverting input. Connect to resolver COS LO.
20	COS	COS channel noninverting input. Connect to resolver COS HI output. COS = 2 V rms ± 10%.

CAUTION

The AD2S90 features an input protection circuit consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charges Device Model).

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. For further information on ESD precautions, refer to Analog Devices *ESD Prevention Manual*.

RESOLVER FORMAT SIGNALS

A resolver is a rotating transformer which has two stator windings and one rotor winding. The stator windings are displaced mechanically by 90° (see Figure 4). The rotor is excited with an ac reference. The amplitude of subsequent coupling onto the stator windings is a function of the position of the rotor (shaft) relative to the stator. The resolver, therefore, produces two output voltages (S3–S1, S2–S4) modulated by the SINE and COSINE of shaft angle. Resolver format signals refer to the signals derived from the output of a resolver. Equation 1 illustrates the output form.

$$S3–S1 = E_O \, SIN\, \omega t \bullet SIN\theta$$
$$S2–S4 = E_O \, SIN\, \omega t \bullet COS\theta \quad (1)$$

where: θ = shaft angle
SIN ωt = rotor excitation frequency
E_O = rotor excitation amplitude

Principle of Operation

The AD2S90 operates on a Type 2 tracking closed-loop principle. The output continually tracks the position of the resolver without the need for external convert and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB.

On the AD2S90, CLKOUT updates corresponding to one LSB increment. If we assume that the current word state of the up-down counter is ϕ, S3–S1 is multiplied by COS ϕ and S2–S4 is multiplied by SIN ϕ to give:

$$E_O \, SIN\, \omega t \bullet SIN\, \theta \, COS\phi$$
$$E_O \, SIN\, \omega t \bullet COS\, \theta \, SIN\phi \quad (2)$$

An error amplifier subtracts these signals giving:

$$E_O \, SIN\, \theta \bullet (SIN\, \theta \, COS\, \phi - COS\, \theta \, SIN\, \phi)$$

or

$$E_O \, SIN\, \omega t \bullet SIN\, (\theta - \phi) \quad (3)$$

where $(\theta - \phi)$ = angular error

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null sin $(\theta - \phi)$. When this is accomplished the word state of the up/down counter, ϕ, equals within the rated accuracy of the converter, the resolver shaft angle θ.

For more information on the operation of the converter, see Circuit Dynamics section.

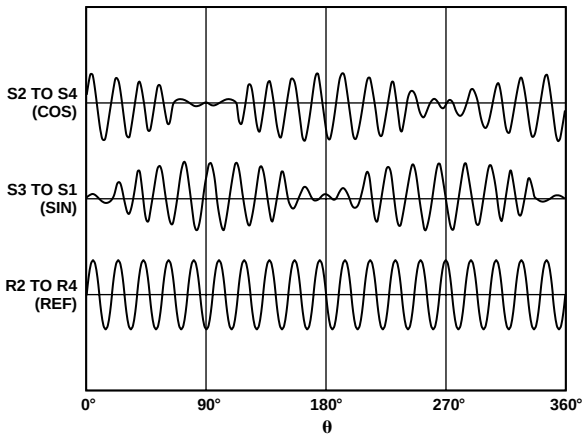


Figure 4. Electrical and Physical Resolver Representation

Connecting The Converter

Refer to Figure 4. Positive power supply V_{DD} = +5 V dc ± 5% should be connected to Pin 13 & Pin 14 and negative power supply V_{SS} = –5 V dc ± 5% to Pin 12. **Reversal of these power supplies will destroy the device.** S3 (SIN) and S2 (COS) from the resolver should be connected to the SIN and COS pins of the converter. S1 (SIN) and S4 (COS) from the resolver should be connected to the SINLO and COSLO pins of the converter. The maximum signal level of either the SIN or COS resolver outputs should be 2 V rms ± 10%. The AD2S90 AGND pin is the point at which all analog signal grounds should be star connected. The SIN LO and COS LO pins on the AD2S90 should be connected to AGND. Separate screened twisted cable pairs are recommended for all analog inputs SIN, COS, and REF. The screens should terminate at the converter AGND pin.

North marker width selection is controlled by Pin 15, NMC. Application of V_{DD}, 0 V, or V_{SS} to NMC will select standard 90°, 180° and 360° pulsewidths. If unconnected, the NM pulse defaults to 90°. For a more detailed description of the output formats available see the Position Output section.

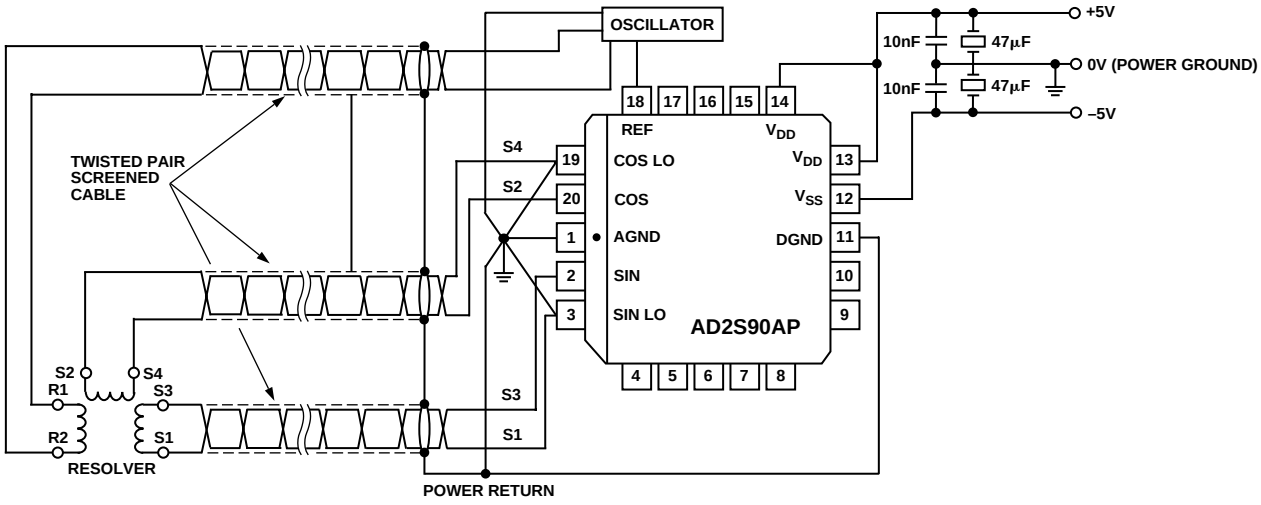


Figure 5. Connecting the AD2S90 to a Resolver

ABSOLUTE POSITION OUTPUT

SERIAL INTERFACE

Absolute angular position is represented by serial binary data and is extracted via a three-wire interface, DATA, $\overline{CS}$ and SCLK. The DATA output is held in a high impedance state when $\overline{CS}$ is HI.

Upon the application of a Logic LO to the $\overline{CS}$ pin, the DATA output is enabled and the current angular information is transferred from the counters to the serial interface. Data is retrieved by applying an external clock to the SCLK pin. The maximum data rate of the SCLK is 2 MHz. To ensure secure data retrieval it is important to note that SCLK should not be applied until a minimum period of 600 ns after the application of a Logic LO to $\overline{CS}$. Data is then clocked out, MSB first, on successive negative edges of the SCLK; 12 clock edges are required to extract the full 12 bits of data. Subsequent negative edges greater than the defined resolution of the converter will clock zeros from the data output if $\overline{CS}$ remains in a low state.

If a resolution of less than 12 bits is required, the data access can be terminated by releasing $\overline{CS}$ after the required number of bits have been read.

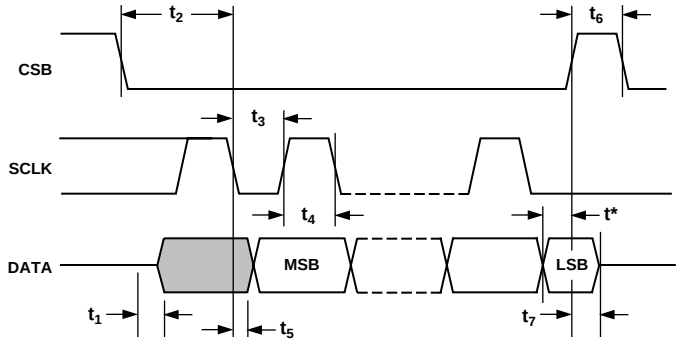


Figure 6. Serial Read Cycle

$\overline{CS}$ can be released a minimum of 100 ns after the last negative edge. If the user is reading data continuously, $\overline{CS}$ can be reapplied a minimum of 250 ns after it is released (see Figure 6).

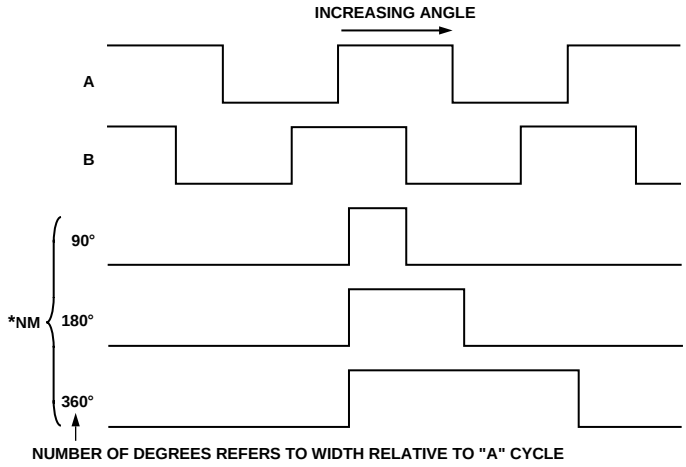
The maximum read time is given by: (12-bits read @ 2 MHz)
Max RD Time = [600 + (12 × 500) + 600 + 100] = 7.30 µs.

INCREMENTAL ENCODER OUTPUTS

The incremental encoder emulation outputs A, B and NM are free running and are always valid, providing that valid resolver format input signals are applied to the converter.

The AD2S90 emulates a 1024-line encoder. Relating this to converter resolution means one revolution produces 1024 A, B pulses. B leads A for increasing angular rotation (i.e., clockwise direction). The addition of the DIR output negates the need for external A and B direction decode logic. DIR is HI for increasing angular rotation.

The north marker pulse is generated as the absolute angular position passes through zero. The AD2S90 supports the three industry standard widths controlled using the NMC pin. Figure 7 details the relationship between A, B and NM. The width of NM is defined relative to the A cycle.



*SELECTABLE WITH THREE - LEVEL CONTROL PIN "MARKER" DEFAULT TO 90° USING INTERNAL PULL - UP.

LEVEL	WIDTH
$+V_{DD}$	90°
0	180°
$-V_{SS}$	360°

Figure 7. A, B and NM Timing

Unlike incremental encoders, the AD2S90 encoder output is not subject to error specifications such as cycle error, eccentricity, pulse and state width errors, count density and phase ϕ.

The maximum speed rating, n, of an encoder is calculated from its maximum switching frequency, f_{MAX}, and its ppr (pulses per revolution).

$$n = \frac{60 \times f_{MAX}}{PPR}$$

The AD2S90 A, B pulses are initiated from CLKOUT which has a maximum frequency of 2.048 MHz. The equivalent encoder switching frequency is:

$$1/4 \times 2.048\ MHz = 512\ kHz\ (4\ updates = 1\ pulse)$$

At 12 bits the ppr = 1024, therefore the maximum speed, n, of the AD2S90 is:

$$n = \frac{60 \times 512000}{1024} = 30000\ rpm$$

This compares favorably with encoder specifications where f_{MAX} is specified from 20 kHz (photo diodes) to 125 kHz (laser based) depending on the light system used. A 1024 line laser-based encoder will have a maximum speed of 7300 rpm.

The inclusion of A, B outputs allows the AD2S90 + resolver solution to replace optical encoders directly without the need to change or upgrade existing application software.

VELOCITY OUTPUT

The analog velocity output VEL is scaled to produce 150 rps/V dc ± 15%. The sense is positive V dc for increasing angular rotation. VEL can drive a maximum load combination of 10 kΩ and 30 pF. The internal velocity scaling is fixed.

POSITION CONTROL

The rotor movement of dc or ac motors used for servo control is monitored at all times. Feedback transducers used for this purpose detect either relative position in the case of an incremental encoder or absolute position and velocity using a resolver. An incremental encoder only measures change in position not actual position.

Closed Loop Control Systems

The primary demand for a change in position must take into account the magnitude of that change and the associated acceleration and velocity characteristics of the servo system. This is necessary to avoid "hunting" due to over- or underdamping of the control employed.

A position loop needs both actual and demand position information. Algorithms consisting of proportional, integral and derivative control (PID) may be implemented to control the velocity profile.

A simplified position loop is shown in Figure 8.

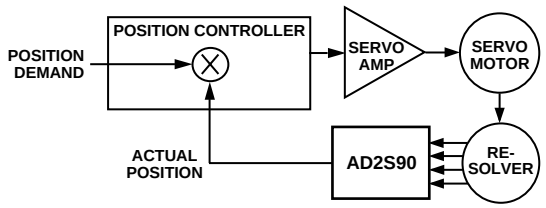


Figure 8. Position Loop

MOTION CONTROL PROCESSES

Advanced VLSI designs mean that silicon system blocks are now available to achieve high performance motion control in servo systems.

A digital position control system using the AD2S90 is shown in Figure 9. In this system the task of determining the acceleration and velocity characteristics is fulfilled by programming a trapezoidal velocity profile via the I/O port.

As can be seen from Figure 9 encoder position feedback information is used. This is a popular format and one which the AD2S90 emulates thereby facilitating the replacement of encoders with an AD2S90 and a resolver. However, major benefits can be realized by adopting the resolver principle as opposed to the incremental technique.

Incremental feedback based systems normally carry out a periodic check between the position demanded by the controller and the increment position count. This requires software and hardware comparisons and battery backup in the case of power failure. If there is a supply failure and the drive system moves, unless all parts of the system are backed up, a reset to a known datum point needs to take place. This can be extremely hazardous in many applications. The AD2S90 gets round this problem by supplying an absolute position serial data stream upon request, thus removing the need to reset to a known datum.

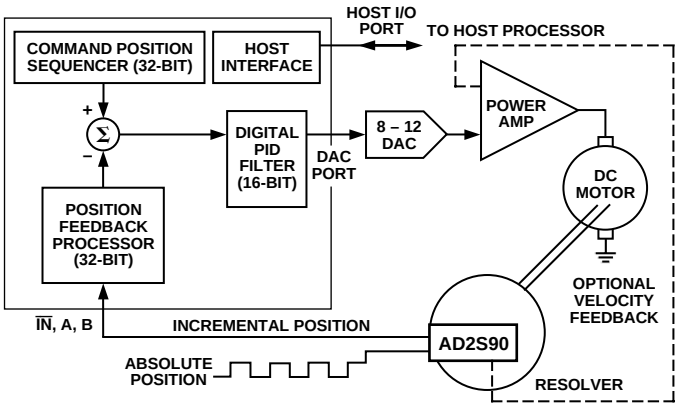


Figure 9. Practical Implementation of the AD2S90

DSP Interfacing

The AD2S90 serial output is ideally suited for interfacing to DSP configured microprocessors. Figures 10 to 13 illustrate how to configure the AD2S90 for serial interfacing to the DSP.

ADSP-2105 Interfacing

Figure 10 shows the AD2S90 interfaced to an ADSP-2105. The on-chip serial port of the ADSP-2105 is used in alternate framing receive mode with internal framing (internally inverted) and internal serial clock generation (externally inverted) options selected. In this mode the ADSP-2105 provides a $\overline{CS}$ and a serial clock to the AD2S90. The serial clock is inverted to prevent timing errors as a result of both the AD2S90 and ADSP-2105 clock data on the negative edge of SCLK. The first data bit is void; 12 bits of significant data then follow on each consecutive negative edge of the clock. Data is clocked from the AD2S90 into the data receive register of the ADSP-2105. This is internally set to 13 bit (12 bits and one "dummy" bit) when 13 bits are received. The serial port automatically generates an internal processor interrupt. This allows the ADSP-2105 to read 12 significant bits at once and continue processing.

The ADSP-2101, ADSP-2102, ADSP-2111 and 21msp50 can all interface to the AD2S90 with similar interface circuitry.

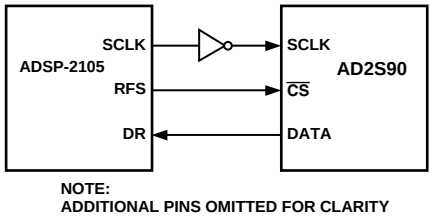


Figure 10. ADSP-2105/AD2S90 Serial Interface

TMS32020 Interfacing

Figure 11 shows the serial interface between the AD2S90 and the TMS32020. The interface is configured in alternate internal framing, external clock (externally inverted) mode. Sixteen bits of data are clocked from the AD2S90 into the data receive register (DRR) of the TMS32020. The DRR is fixed at 16 bits. To obtain the 12-significant bits, the processor needs to execute three right shifts. (First bit read is void, the last three will be zeros). When 16 bits have been received by the TMS32020, it generates an internal interrupt to read the data from the DRR.

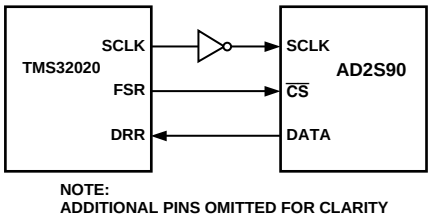


Figure 11. TMS32020/AD2S90 Serial Interface

DSP56000 Interface

Figure 12 shows a serial interface between the AD2S90 and the DSP56000. The DSP in configured for normal mode synchronous operation with gated clock with SCLK and SC1 as outputs. SC1 is applied to $\overline{CS}$.

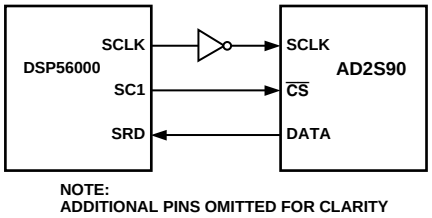


Figure 12. DSP56000/AD2S90 Serial Interface

The DSP56000 assumes valid data on the first falling edge of SCLK. SCLK is inverted to ensure that the valid data is clocked in after one leading bit. The receive data shift register (SRD) is set for a 13-bit word.

When this register has received 13 bits of data, it generates an internal interrupt on the DSP56000 to read the 12 bits of significant data from the register.

NEC7720 Interface

Figure 13 shows the serial interface between the NEC7720 and the AD2S90. The NEC7720 expects data on the rising edge of its SCLK output, and therefore unlike the previous interfaces no inverter is required to clock data into the S1 register. There is no need to ignore the first data bit read. $\overline{SIEN}$ is used to Chip Select the AD2S90 and frame the data. The S1 register is fixed at 16 bits, therefore, to obtain the 12-significant bits the processor needs to execute four right shifts. Once the NEC7720 has read 16 bits, an internal interrupt is generated to read the internal contents of the S1 register.

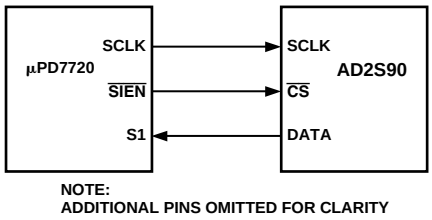


Figure 13. µPD7720/AD2S90 Serial Interface

EDGE TRIGGERED 4× DECODING LOGIC

In most data acquisition or control systems the A, B incremental outputs must be decoded into absolute information, normally a parallel word, before they can be utilized effectively.

To decode the A, B outputs on the AD2S90 the user must implement a 4× decoding architecture. The principle states that one A, B cycle represents 4 LSB weighted increments of the converter (see Equation 4).

$$Up = (\uparrow A) \bullet B + (\downarrow B) \bullet A + (\downarrow A) \bullet \overline{B} + (\uparrow B) \bullet \overline{A}$$
$$Down = (\uparrow A) \bullet \overline{B} + (\uparrow B) \bullet A + (\downarrow A) \bullet B + (\downarrow B) \bullet \overline{A} \quad (4)$$

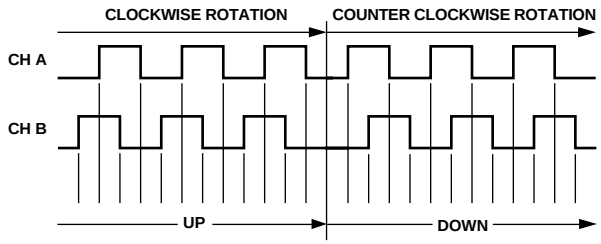


Figure 14. Principles of 4× Decoding

The algorithms in Equation 4 can be implemented using the architecture shown in Figure 15. Traditionally the direction of the shaft is decoded by determining whether A leads B. The AD2S90 removes the need to derive direction by supplying a direction output state which can be fed straight into the up-down counter.

For further information on this topic please refer to the application note "Circuit Applications of the AD2S90 Resolver-to-Digital Converters."

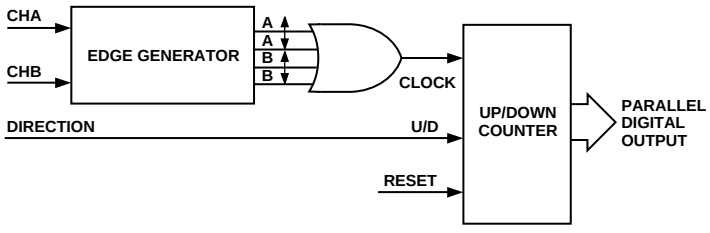


Figure 15. 4× Decoding Incremental to Parallel Conversion

REMOTE MULTIPLE SENSOR INTERFACING

The DATA output of the AD2S90 is held in a high impedance state until $\overline{CS}$ is taken LO. This allows a user to operate the AD2S90 in an application with more than one converter connected on the same line. Figure 16 shows four resolvers interfaced to four AD2S90s. Excitation for the resolvers is provided locally by an oscillator.

SCLK, DATA and two address lines are fed down low loss cables suitable for communication links. The two address lines are decoded locally into $\overline{CS}$ for the individual converters. Data is received and transmitted using transmitters and receivers.

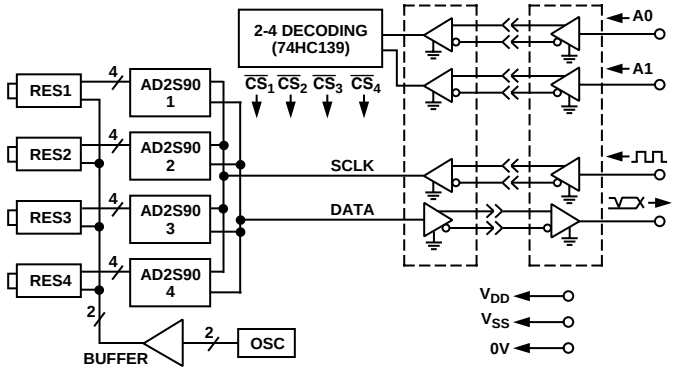


Figure 16. Remote Sensor Interfacing

CIRCUIT DYNAMICS/ERROR SOURCES

Transfer Function

The AD2S90 operates as a Type 2 tracking servo loop. An integrator and VCO/counter perform the two integrations inherent in a Type 2 loop.

The overall system response of the AD2S90 is that of a unity gain second order low-pass filter, with the angle of the resolver as the input and the digital position data as the output. Figure 17 illustrates the AD2S90 system diagram.

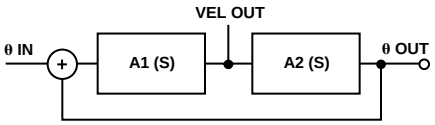


Figure 17. AD2S90 Transfer Function

The open-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1 K_2}{s^2}\frac{(1+st_1)}{1+st_2} \tag{5}$$

where:

$$A_1(s) = \frac{K_1}{s}\frac{1+st_1}{1+st_2} \qquad \begin{matrix} t_1 = 1.0\,ms \\ t_2 = 90\,\mu s \end{matrix} \tag{6}$$

$$A_2(s) = \frac{K_2}{s} \qquad \begin{matrix} K_1 = 4.875 V/(LSB \times \sec) \\ K_2 = 614{,}400\,LSB/(V \times \sec) \end{matrix} \tag{7}$$

The AD2S90 acceleration constant is given by:

$$K_a = K_1 \times K_2 \cong 3.0 \times 10^6 \sec^{-2} \tag{8}$$

The AD2S90's design has been optimized with a critically damped response. The closed-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1+st_1}{1+st_1+\frac{s^2}{K_1K_2}+\frac{s^3t_2}{K_1K_2}} \tag{9}$$

The normalized gain and phase diagrams are given in Figures 18 and 19.

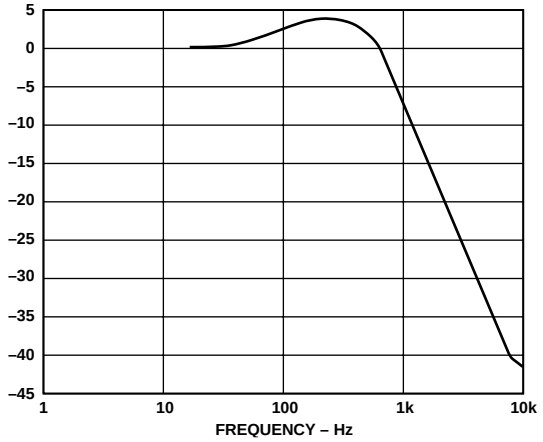


Figure 18. AD2S90 Gain Plot

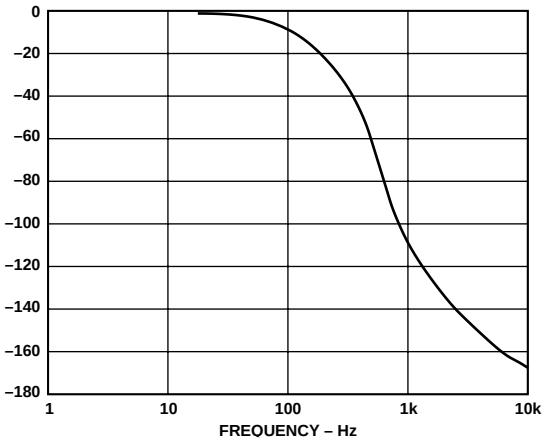


Figure 19. AD2S90 Phase Plot

The small step response is given in Figure 20, and is the time taken for the converter to settle to within 1 LSB.

ts = 7.00 ms (maximum)

The large step response (steps >20°) applies when the error voltage will exceed the linear range of the converter. Typically it will take three times longer to reach the first peak for a 179° step.

In response to a velocity step [VELOUT/(dθ/dt)] the velocity output will exhibit the same response characteristics as outlined above.

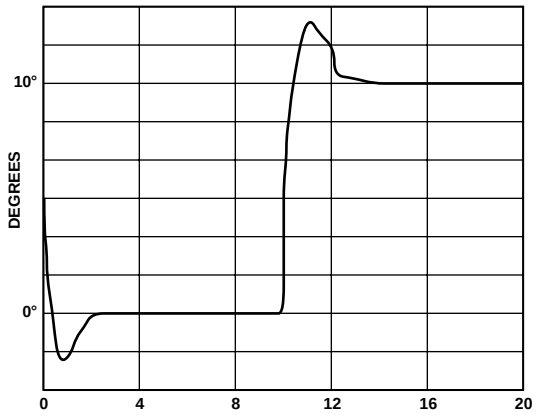


Figure 20. Small Step Response

SOURCES OF ERROR

Acceleration Error

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{Input\ Acceleration}{Error\ in\ Output\ Angle} \tag{10}$$

The numerator and denominator's units must be consistent. *K_a does not define maximum input acceleration,* only the error due to its acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$Angular\ Error \times K_a = degrees/sec^2 \tag{11}$$

K_a can be used to predict the output position error for a given input acceleration. The AD2S90 has a fixed $K_a = 3.0 \times 10^6$ sec^{-2} if we apply an input accelerating at 100 revs/sec^2, the error can be calculated as follows:

$$Error\ in\ LSBs = \frac{Input\ Acceleration\ \left[LSB/sec^2\right]}{K_a\left[sec^{-2}\right]}$$

$$= \frac{100\left[rev/\sec^2\right] \times 2^{12}\left[LSB/rev\right]}{3.0 \times 10^6\left[\sec^{-2}\right]} = 0.14\ LSBs \tag{12}$$

AD2S90/AD2S99 TYPICAL CONFIGURATION

Figure 21 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S90 Resolver-to-Digital Converter. The maximum level of the SIN and COS input signals to the AD2S90 should be 2 V rms ±10%. All the analog ground signals should be star connected to the AD2S90 AGND pin. If shielded twisted pair cables are used for the resolver signals, the shields should also be terminated at the AD2S90 AGND pin. The SYNREF output of the AD2S99 should be connected to the REF input pin of the AD2S90 via a 0.1 μF capacitor with a 100 kΩ resistor to GND. This is to block out any dc offset in the SYNREF signal. For more detailed information please refer to the AD2S99 data sheet.

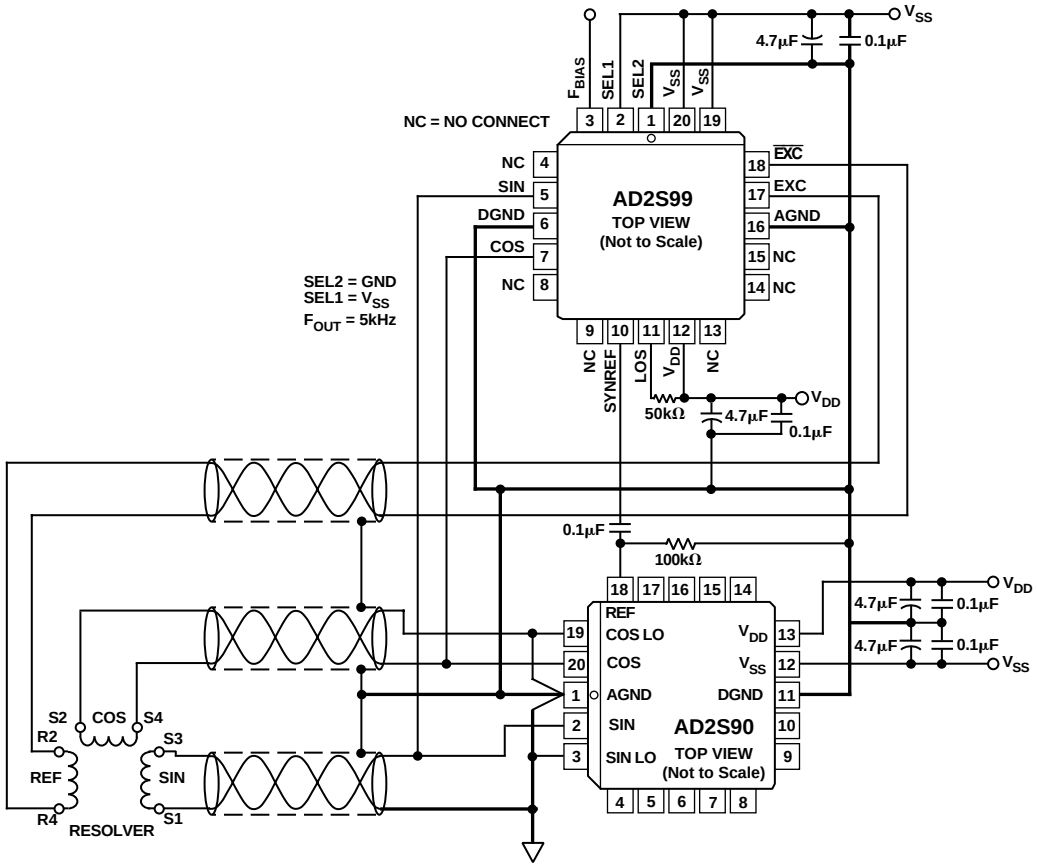
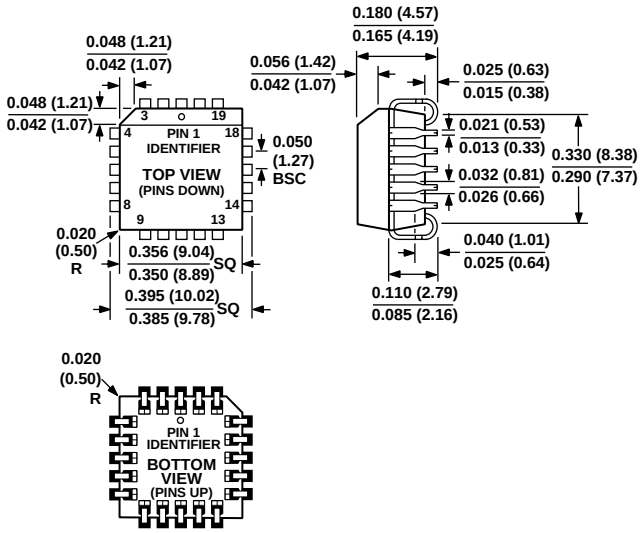


Figure 21. AD2S90 and AD2S99 Example Configuration

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

P-20A
20-Lead Plastic Leaded Chip Carrier (PLCC)



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